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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,094	CHAN ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16 and 18-20* is/are rejected.

7)☒ Claim(s) *2 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The examiner is unsure of the metes and bounds of claims 7-10. These claims are dependent upon claim 1, but in view of the other claims which are dependent upon claim 1, the examiner believes that claims 7-10 should be dependent on claim 6. Furthermore this discrepancy has also lead to antecedent basis problems and double patenting warnings which are discussed below.

4. Claim 7 recites the limitation "the sidewall spacer" in line 1. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 10 recites the limitation "the ultra-uniform silicide" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 3, 5, 11, 13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Iinuma (USPN 6,770,942 B2).

8. In reference to claims 1, 3, and 11, Iinuma (USPN 6,770,942 B2) discloses a similar device and its method of fabrication. Figures 1-8 of Iinuma illustrate an integrated circuit with a gate dielectric layer (12) on a semiconductor substrate (1). There is a gate (13) with silicide (14a) on the gate dielectric layer (12). There are source/drain junctions (21) with silicide (14b) in the semiconductor substrate (1). There are trenches in the semiconductor substrate (1) around the gate (13). Iinuma makes it clear (column 2, lines 25-29 and in figure 2) that the trenches are formed by an etching process that etches a semiconductor substrate (1). There is an interlayer dielectric (31) above the semiconductor substrate (1). There are contacts (32) to the source/drain junctions (21).

9. With regard to claim 13, the trenches extend into the semiconductor substrate (1) to a level lower than the silicide (14b).

10. In reference to claims 5 and 15, Iinuma discloses (column 4, lines 60-62) the use of copper for the contact material (32).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 3, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141).

13. In reference to claims 1, 3, and 11, Kang et al. (USPN 5,665,990, hereinafter referred to as the "Kang" reference) discloses a similar device and its method of fabrication. Figures 3-5 of Kang each illustrate an integrated circuit with a gate dielectric layer on a semiconductor substrate (1). Figures 2A-2D illustrate the basic process for fabricating the devices of figures 3-5. There is a gate (4) on the gate dielectric layer. There are source/drain junctions (7) in the semiconductor substrate (1). There are trenches in the semiconductor substrate (1) around the gate (4). Kang makes it clear (column 3, lines 49-54 and in figures 2A-2D) that the trenches are formed by an etching process that etches a semiconductor substrate (1). There is an interlayer dielectric above the semiconductor substrate (1). There are contacts to the source/drain junctions (7). Kang does not disclose the use of a silicide with the source/drain junctions (7) however the use of silicides is well known in the art. Merrill (USPN 5,918,141) illustrates a device which uses a silicide layer with the source/drain junctions and the gate in figures 1A-1E. Furthermore Merrill discloses that using

a silicide reduces contact resistance which leads to the benefit of a high speed device (column 1, lines 15-27). In view of Merrill, it would therefore be obvious to use silicide with the source/drain junctions and gate in the device of Kang.

14. With regard to claim 12, there is a sidewall spacer (8) around the gate (4) wherein the trenches are at the outer edge of the sidewall spacer (8).

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 1 above and further in view of Russell et al. (USPN 5,648,175).

16. In reference to claim 4, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Kang does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell et al. (USPN 5,648,175, hereinafter referred to as the "Russell" reference) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 1 above and further in view of Sekiguchi (USPN 6,333,255 B1).

18. In reference to claim 4, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Kang does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 1 above and further in view of Liauh (USPN 5,027,185) and further in view of Wald et al. (USPN 5,932,491).

20. In reference to claim 5, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Wald et al. (USPN 5,932,491, hereinafter referred to as the "Wald" reference) discloses the use of titanium, tungsten, and alloys thereof in a contact since they have a low resistance (column 5, lines 45-48). In view of Liauh and Wald, it would therefore

be obvious to use titanium, tungsten, and its alloys as contacts in order to gain the benefit of a low resistance contact.

21. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 1 above and further in view of Liauh (USPN 5,027,185) and further in view of Yoshida et al. (USPN 6,580,143 B2).

22. In reference to claim 5, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Yoshida et al. (USPN 6,580,143 B2, hereinafter referred to as the "Yoshida" reference) discloses that gold, silver, and titanium have a low resistance (column 4, lines 11-16). In view of Liauh and Yoshida, it would therefore be obvious to gold, silver, and titanium as contacts in order to gain the benefit of a low resistance contact.

23. Claims 6, 8, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141).

24. In reference to claims 6, 8, and 16, Kang (USPN 5,665,990) discloses a similar device and its fabrication method. Figures 3-5 of Kang each illustrate an integrated circuit with a gate dielectric layer on a semiconductor substrate (1). Figures 2A-2D illustrate the basic process for fabricating the devices of figures 3-5. There is a gate (4) on the gate dielectric layer. There are source/drain

junctions (7) in the semiconductor substrate (1). There is a sidewall spacer (8) around the gate. There are trenches in the semiconductor substrate (1) at the outer edge of the sidewall spacer (8). Kang makes it clear (column 3, lines 49-54 and in figures 2A-2D) that the trenches are formed by an etching process that etches a semiconductor substrate (1). There is an interlayer dielectric above the semiconductor substrate (1). There are contacts to the source/drain junctions (7). Kang does not disclose the use of a silicide with the source/drain junctions (7) however the use of silicides is well known in the art. Merrill (USPN 5,918,141) illustrates a device which uses a silicide layer with the source/drain junctions and the gate in figures 1A-1E. Furthermore Merrill discloses that using a silicide reduces contact resistance which leads to the benefit of a high speed device (column 1, lines 15-27). In view of Merrill, it would therefore be obvious to use silicide with the source/drain junctions and gate in the device of Kang.

25. With regard to claim 18, Kang and Merrill teach all of the claimed invention except for the exact trench depth. Although the Kang and Merrill references do not teach the exact trench depths that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 18 is not patentably distinguishable over the Kang and Merrill references.

26. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 6 above and further in view of Russell et al. (USPN 5,648,175).

27. So far as understood in claim 9, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Figures 2A-2D illustrate the basic process for fabricating the devices of figures 3-5. Kang does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell (USPN 5,648,175) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

28. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 6 above and further in view of Sekiguchi (USPN 6,333,255 B1).

29. So far as understood in claim 9, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Figures 2A-2D illustrate the basic process for fabricating the devices of figures 3-5. Kang does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal

in the art (column 1, lines 10-15). In view of Sekiguchi, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

30. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 6 above and further in view of Liauh (USPN 5,027,185) and further in view of Wald et al. (USPN 5,932,491).

31. So far as understood in claim 10, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Wald et al. (USPN 5,932,491, hereinafter referred to as the "Wald" reference) discloses the use of titanium, tungsten, and alloys thereof in a contact since they have a low resistance (column 5, lines 45-48). In view of Liauh and Wald, it would therefore be obvious to use titanium, tungsten, and its alloys as contacts in order to gain the benefit of a low resistance contact.

32. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 6 above and further in view of Liauh (USPN 5,027,185) and further in view of Yoshida et al. (USPN 6,580,143 B2).

33. So far as understood in claim 10, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang

does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Yoshida et al. (USPN 6,580,143 B2, hereinafter referred to as the "Yoshida" reference) discloses that gold, silver, and titanium have a low resistance (column 4, lines 11-16). In view of Liauh and Yoshida, it would therefore be obvious to gold, silver, and titanium as contacts in order to gain the benefit of a low resistance contact.

34. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 11 above and further in view of Russell et al. (USPN 5,648,175).

35. In reference to claim 14, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Kang does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell (USPN 5,648,175) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

36. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 11 above and further in view of Sekiguchi (USPN 6,333,255 B1).

37. In reference to claim 14, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Kang does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

38. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 11 above and further in view of Liauh (USPN 5,027,185) and further in view of Wald et al. (USPN 5,932,491).

39. In reference to claim 15, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Wald et al. (USPN

5,932,491, hereinafter referred to as the "Wald" reference) discloses the use of titanium, tungsten, and alloys thereof in a contact since they have a low resistance (column 5, lines 45-48). In view of Liauh and Wald, it would therefore be obvious to use titanium, tungsten, and its alloys as contacts in order to gain the benefit of a low resistance contact.

40. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 11 above and further in view of Liauh (USPN 5,027,185) and further in view of Yoshida et al. (USPN 6,580,143 B2).

41. In reference to claim 15, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Yoshida et al. (USPN 6,580,143 B2, hereinafter referred to as the "Yoshida" reference) discloses that gold, silver, and titanium have a low resistance (column 4, lines 11-16). In view of Liauh and Yoshida, it would therefore be obvious to gold, silver, and titanium as contacts in order to gain the benefit of a low resistance contact.

42. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 16 above and further in view of Russell et al. (USPN 5,648,175).

43. In reference to claim 19, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Kang does not explicitly disclose the

use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell (USPN 5,648,175) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

44. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 16 above and further in view of Sekiguchi (USPN 6,333,255 B1).

45. In reference to claim 19, figures 3-5 of Kang each illustrate an integrated circuit which uses an interlayer dielectric. Kang does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Kang in order to attain these benefits.

46. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 16 above and further in view of Liauh (USPN 5,027,185) and further in view of Wald et al. (USPN 5,932,491).

47. In reference to claim 20, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Wald et al. (USPN 5,932,491, hereinafter referred to as the "Wald" reference) discloses the use of titanium, tungsten, and alloys thereof in a contact since they have a low resistance (column 5, lines 45-48). In view of Liauh and Wald, it would therefore be obvious to use titanium, tungsten, and its alloys as contacts in order to gain the benefit of a low resistance contact.

48. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990) in view of Merrill (USPN 5,918,141) as applied to claim 16 above and further in view of Liauh (USPN 5,027,185) and further in view of Yoshida et al. (USPN 6,580,143 B2).

49. In reference to claim 20, figures 3-5 of Kang each illustrate an integrated circuit which uses a contact for the source/drain junctions (7). Kang does not disclose the exact material which is used for the contact. However Liauh (USPN 5,027,185) discloses that in the semiconductor art, contacts are formed with low resistance as a desired goal (column 1, lines 38-57). Yoshida et al. (USPN

6,580,143 B2, hereinafter referred to as the "Yoshida" reference) discloses that gold, silver, and titanium have a low resistance (column 4, lines 11-16). In view of Liauh and Yoshida, it would therefore be obvious to gold, silver, and titanium as contacts in order to gain the benefit of a low resistance contact.

50. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iinuma (USPN 6,770,942 B2) in view of Russell et al. (USPN 5,648,175).

51. In reference to claim 4, figures 1-8 of Iinuma illustrate an integrated circuit which uses an interlayer dielectric (31). Iinuma does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell (USPN 5,648,175) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Iinuma in order to attain these benefits.

52. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iinuma (USPN 6,770,942 B2) in view of Sekiguchi (USPN 6,333,255 B1).

53. In reference to claim 4, figures 1-8 of Iinuma illustrate an integrated circuit which uses an interlayer dielectric (31). Iinuma does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for

use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Iinuma in order to attain these benefits.

54. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iinuma (USPN 6,770,942 B2) in view of Russell et al. (USPN 5,648,175).

55. In reference to claim 14, figures 1-8 of Iinuma illustrate an integrated circuit which uses an interlayer dielectric (31). Iinuma does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such a material is well known in the art. Russell (USPN 5,648,175) discloses that BPSG (borophosphosilicate glass) is desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant, low stress, and good adhesion properties (column 1, lines 27-30). Russell discloses that these qualities are desirable in the art (column 1, lines 41-44). In view of Russell, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Iinuma in order to attain these benefits.

56. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iinuma (USPN 6,770,942 B2) in view of Sekiguchi (USPN 6,333,255 B1).

57. In reference to claim 14, figures 1-8 of Iinuma illustrate an integrated circuit which uses an interlayer dielectric (31). Iinuma does not explicitly disclose the use of a low dielectric constant interlayer dielectric. However the use of such

a material is well known in the art. Sekiguchi (USPN 6,333,255 B1) discloses that low dielectric constant materials, such as HSQ and Teflon-AF, are desirable for use as an interlayer dielectric since it has the benefits of a low dielectric constant which leads to the possibility of a smaller device (column 1, lines 35-46). The attainment of a smaller semiconductor device is a known goal in the art (column 1, lines 10-15). In view of Sekiguchi, it would therefore be obvious to use a low dielectric constant interlayer dielectric in the device of Iinuma in order to attain these benefits.

Double Patenting

58. Applicant is advised that should claim 3 be found allowable, claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

59. Applicant is advised that should claim 4 be found allowable, claim 9 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

60. Claims 2 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

61. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a field effect transistor having a silicided gate, as well as silicided source and drain regions, with multi-layer spacers which have an outer edge which is aligned with the sidewall of a trench.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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KVQ